Self-assembly of periodic nanoclusters of Si and Ge along atomically straight steps of a vicinal Si(111)[*]

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The very initial stage of the molecular beam epitaxy of Si and Ge on Si(111)-7×7 substrates with atomically straight steps has been studied by scanning tunneling microscopy and spectroscopy. The atomically straight steps have been prepared on a miscut Si(111) substrate by annealing at 830 °C with kink-up direct current. The length of the steps can be maximized by selecting a proper annealing time. The steps have a well-defined $U(2, 0)$ step-edge structure. The growth of both Si and Ge at temperatures between 250 and 400 °C starts with formation of a single-adatom-row nanowire (0.67 nm in width) along the lower edge of each $U(2, 0)$ step. Subsequent growth of Si and Ge at temperatures between 250 and 300 °C results in formation of one-dimensional arrays of nanoclusters (less than 2.0 nm in width) in the unfaulted halves of the 7×7 structure along the upper step edges. Scanning tunneling spectroscopy reveals localized electronic states of the nanoclusters. Differences between the growth of Si and Ge nanoclusters are discussed. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2722726]

I. INTRODUCTION

Self-assembly of ordered nanostructures on semiconductor surfaces has been extensively studied. Especially the Ge/Si system is important as a model of the heteroepitaxial Stranski–Krastanow growth, in which strained three-dimensional islands of nanoscale dimensions are self-organized.[1–3] Quantum confinement effect in these islands is useful for optoelectronic device applications based on the Si technology.[3–15] The homoepitaxial Si/Si growth is also important because isotopically controlled Si structures are expected to serve as building blocks of novel application devices, such as a quantum computer utilizing Si nuclear spin.[16]

Himpsel and co-workers have experimentally demonstrated that vicinal Si(111) surfaces can serve as templates for self-assembly of one-dimensional (1D) nanostructures,[17,18] because a regular array of straight steps can be obtained on these surfaces.[19–21] Improving their method of the straight-step preparation by substrate annealing with step-parallel direct current (dc), we have found that the "kink-up" direction (ascending kinks of the steps) of the dc is effective to obtain atomically straight step edges (on the

order of 1 μm in length) probably due to electromigration of the surface atoms.[22] We have studied the growth behavior of Si (Ref. 23) and Ge (Ref. 24) on this straight-step substrate and found the formation of characteristic nanostructures.

The present article reports a unified picture of the growth of the Si and Ge nanostructures on the straight-step Si(111) substrate. After describing the experimental methods used in this study, we observe the step morphology evolution during annealing to find the optimum annealing time for preparing the straight steps. Then, we compare the initial growth behavior of Si and Ge nanostructures at several substrate temperatures in detail. We describe the results of a scanning tunneling spectroscopy (STS) study that reveals localized electronic states of Ge nanoclusters.

II. EXPERIMENTAL PROCEDURES

To prepare highly ordered stepped substrates of Si(111), we used the method described in Ref. 22. Small pieces ($0.65\times3\times13$ mm^3) of a nominal (111) Si wafer were polished to make miscut of $\theta\approx1°$ toward the $[\bar{1}12]$ direction with the intentional azimuthal misorientation of $\phi\approx3°$. These vicinal substrates were introduced into an ultrahigh vacuum chamber and heated by passing dc current in the kink-up direction, in the following sequences. First, the substrates were cleaned with flash heating up to 1300 °C followed by quenching to room temperature within 3 s. Then, the substrates were annealed at 830 °C, followed by very slow cool-down to room temperature. Particularly in this study we varied the annealing time t_a at 830 °C, to find the optimum for the step straightening. After each of these step-preparation processes and the subsequent growth processes, the surface structure was measured by scanning tunneling

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microscopy (STM) *in situ* at room temperature.

We deposited Si and Ge atoms from molecular beam epitaxy sources onto the substrates with optimally extended straight steps. The Si source was an effusion cell with a tantalum crucible and the Ge sources were an effusion cell with a boron-nitride crucible (structural study) and an electron beam evaporator (STS study). The deposition rate (R) and the substrate temperature (T_s) were determined in the same manner as described in Refs. 22–24. The deposition rates used in this study range from 8.9×10^{-4} to 5.0×10^{-2} BL/min dependent on the sources, where 1 BL is the biatomic layer of Si and Ge on the Si(111) surface (equivalent to the density of atoms of 1.57×10^{15} cm^{-2}). In this article, the deposited amount is described with the nominal step coverage (w_x; x=Si or Ge) or with the average film thickness in BL (Θ_x), which is equivalent to the relative area covered with 1 BL islands. We define the step coverage as the width of 1 BL step decoration grown in the step-flow growth mode. The relation between these two notations is $\Theta_x = w_x/W$, where W is the average terrace width.

III. RESULTS AND DISCUSSION

A. Optimum annealing time for the straight step extension

Figure 1 shows the evolution of the step morphology with the annealing time t_a at 830 °C. On the as-cleaned surface quenched from 1300 °C [Fig. 1(a)], almost all the steps are 1 BL high and they have many kinks. All the kinks are oriented in the same direction due to the sufficient azimuthal miscut ($\phi \approx 3°$). Thus, the kink-up direction for the dc annealing is unambiguously defined. If ϕ is below 1°, also the kinks oriented in the opposite direction are formed due to the thermal fluctuation and due to residual surface curvature after the polishing,[22] and the kink-up direction cannot be defined.

After the annealing for t_a=1 h [Fig. 1(b)], the kinks accumulate to form "kink bunches" of up to several BL height. By increasing the annealing time t_a to 2 h [Fig. 1(c)], 6 h [Fig. 1(d)], and 10 h [Fig. 1(e)], the kink bunches become self-aligned in the miscut direction and the straight-step regions are extended up to a few micrometers between the regions of the aligned kink bunches. Additionally, on the 6 and 10 h annealed surfaces, few small kinks oriented in the opposite direction are seen in the straight-step region. Further increase of t_a to 30 h [Fig. 1(f)] leads to formation of oppositely oriented kink bunches, which results in shortening of the straight steps. Thus, we choose the annealing time of 10 h for this sample ($\theta \approx 1°$ and $\phi \approx 3°$) to obtain the most extended straight-step regions.[22–24]

The single steps in the straight-step regions obtained with this annealing process have an identical atomic structure. A STM image of this structure is shown in Fig. 2(a), and its cross section is schematically illustrated in Fig. 2(f). The upper edge of the step is terminated just at the boundaries of the unfaulted halves of the 7×7 structure, as indicated by the triangle. However, at the lower step edge there is an incomplete 7×7 structure, which we call the transition region (TR). The 7×7 structure has a phase shift across the
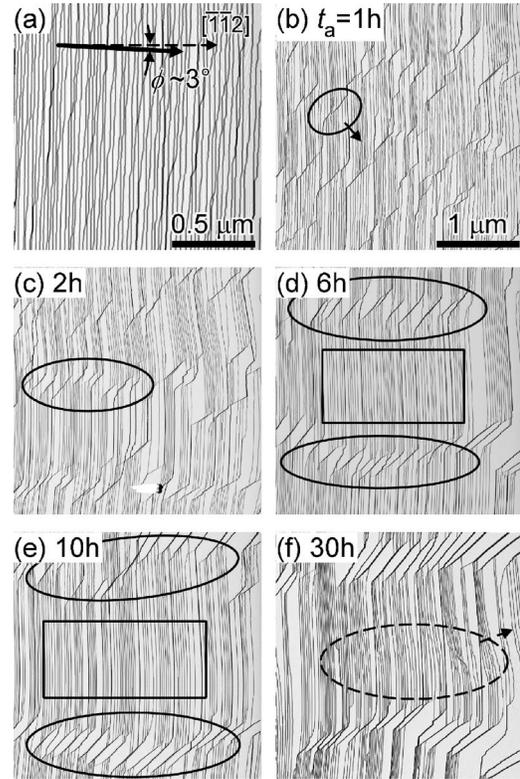

FIG. 1. Differential STM images of the vicinal Si(111) substrate (θ=1.0°) at room temperature. (a) Quenched from 1300 °C, before the annealing at 830 °C. (b)–(f) Slowly cooled down after annealing at 830 °C with kink-up dc current. The annealing times t_a are (b) 1, (c) 2, (d) 6, (e) 10, and (f) 30 h. The scales of the images (b)-(f) are the same, but that of the image (a) is half of them, to make small kinks visible. The thick solid arrow in (a) indicates the average step-down direction that deviates by $\phi \approx 3°$ from the [$\overline{1}\overline{1}2$] direction (the dashed arrow). Kink bunches enclosed by ellipses in (b)–(e) are oriented in the direction of the arrow in (b). Straight-step regions enclosed by rectangles in (d) and (e) are oriented in the [$\overline{1}\overline{1}2$] direction. Kink bunches enclosed by a dashed ellipse in (f) are oriented in the opposite direction indicated by the dashed arrow.

step. The positions of the adatoms in the STM image indicate that this shift is perpendicular to the step and 0.89 nm=(2 +2/3)b in length. b=0.33 nm=$a \sin 60°$, where a =0.384 nm is the interatomic distance on the Si(111) 1×1 unit cell. Thus, the step configuration is $U(2, 0)$.[25] Additionally, the adatom arrangement in the transition region suggests that there is no stacking fault. This unfaulted transition region plays an important role in the growth of Si and Ge as shown later.

B. Si and Ge growth

At high temperatures such as 700 °C, the growth of Si (Ref. 23) and Ge on the atomically straight steps proceeds in the standard step-flow mode. Figure 2(b) shows an STM image of the straight-step region after Si deposition of the step coverage w_{Si}=b at the substrate temperature T_s=700 °C. Before the deposition, the number of kinks is negligible apart from the kink bunch regions and the scarcely observed kinks are oriented in the direction defined by the azimuthal miscut. Therefore, in Fig. 2(b), the step section bounded by the two oppositely oriented kinks must have been formed during the Si deposition. The step propagated by the width of the 7
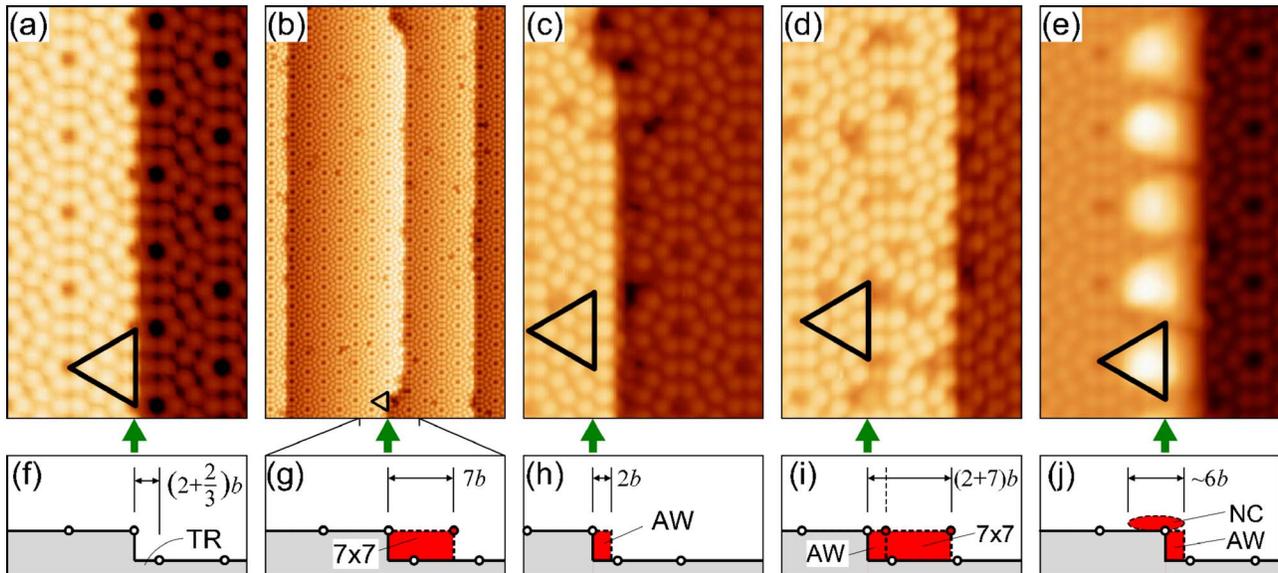
FIG. 2. (Color online) The substrate step-edge structure and the self-assembled structures along it. (a) STM image of the step edge on the 10 h annealed substrates ($\theta=1.0°$). (b)–(e) STM images after the growth of Si at various conditions, on a similarly prepared substrate ($\theta=0.75°$): (b) $T_s=700$ °C with deposited amount of Si $w_{Si}=b(\Theta_{Si}=0.014$ BL); (c) and (d) $T_s=400$ °C with $w_{Si}=7b(\Theta_{Si}=0.097$ BL); (e) $T_s=300$ °C with $w_{Si}=7b(\Theta_{Si}=0.097$ BL). (f)–(j) Schematic cross sections of the STM images (a)–(e). The scales of the images are the same except for the image (b), which is four times lager in length, to show widely separate kinks. The triangle in each image indicates one of the unfaulted halves of the 7×7 structure directly at the upper step edge before the growth. The position of this step edge is additionally marked by a thick (green) arrow. In the cross sections, the substrate and the grown structure are indicated by a light gray body with solid-line surface and by a dark (red) body with dashed-line surface, respectively. The terraces are simplified as horizontal lines with small dots, which indicate the lines connecting corner holes and dimers of the 7×7 structure. The nanocluster is illustrated as an ellipse. The labels (TR, 7×7, AW, and NC) indicate the transition region, the 7×7 extension, the atomic wire, and the nanoclusters, respectively.

$\times7$ half unit cell ($7b$), however, only on a limited length because the nominal step coverage is smaller than the propagation width: $w_{Si}=b<7b$. Because the new step edge is terminated at the unfaulted-half boundaries of the 7×7 structure, the $U(2,0)$ structure of the original step edge is preserved at the new step edge. This step-flow growth is illustrated as a schematic cross section of the step edge in Fig. 2(g). Ge shows the same growth behavior at the same T_s and w. Further deposition of Si and Ge will continue this step-flow growth.

Lowering T_s below 400 °C leads to a different growth behavior.[23,24] At the very beginning of Si and Ge growth ($b\leq w_{Si,Ge}\leq7b$), a characteristic atomic wire structure is formed as an extension of the step edges at 300 °C$\leq T_s$ ≤400 °C for Si and at 250 °C$\leq T_s\leq400$ °C for Ge. Figure 2(c) shows a typical STM image of such wire ($w_{Si}=7b$ and $T_s=400$ °C). A single row of adatoms is formed at the lower edge of the original step. It can be clearly seen because the upper edge of the well-defined step structure $U(2,0)$ before the growth is terminated at the unfaulted half boundaries as indicated by the triangle. The adatoms are regularly arranged with the distance of the adatoms within the 7×7 half-unit cell, $2a=0.77$ nm. The width of the wire is the same as the adatom distance across the half-unit cell boundary, $2b=0.67$ nm. The growth of the atomic wire is restricted to the transition region (0.89 nm in width), as shown schematically in Fig. 2(h). This restriction happens due to the fact that the transition region on the lower terrace has no stacking fault, which makes it structurally different from the normal 7×7 structure next to it.

The growth of Si and Ge after the formation of the atomic wire is more sensitive to the growth temperature T_s.

At $T_s=400$ °C, both Si (Ref. 23) and Ge (Ref. 24) form a 7×7-like decoration next to the atomic wire. The decoration contains many defects. As a result, the local grown width becomes $(2+7)b=3.0$ nm. At the same time, no nucleation is observed on the terraces both for Si and Ge growth. A STM image of the homoepitaxial case ($w_{Si}=7b$ and $T_s=400$ °C) is shown in Fig. 2(d) and its cross section is schematically illustrated in Fig. 2(i). The high density of defects is attributed to the presence of the stacking fault in the underlying 7×7 structure that is difficult to overgrow.[26] Therefore, 400 °C is high enough temperature for the deposited Si and Ge atoms to migrate on the 7×7 terrace and to reach the step edges, though not enough to fully rebuild the stacking fault of the 7×7 structure.

In contrast to the previous scenario, at $T_s\leq300$ °C both Si (Ref. 23) and Ge (Ref. 24) form nanoclusters on the upper edges of the steps after the atomic wire formation. Figure 2(e) shows a STM image of the homoepitaxial case (w_{Si} $=7b$ and $T_s=300$ °C). Nanoclusters are self-assembled on the upper step edge with an adjacent atomic wire. Interestingly, these nanoclusters are not formed at the step edges without the atomic wire and their growth is restricted on the atomic wire and on the unfaulted halves just at the upper step edge. As a result, the nanoclusters are smaller than $6b$ $=2.0$ nm in width as illustrated in Fig. 2(j) and form a simple 1D lattice with periodicity of $7a=2.67$ nm. It was reported that the preferential nucleation site of various atoms on wide 7×7 terraces of the Si(111) surface is the faulted half.[27–31] Therefore, the confinement of the nanoclusters on the unfaulted half in the present study results from the presence of the decorated step edge: The nucleation at the upper step edge is initiated by the atomic wire, which, together with the
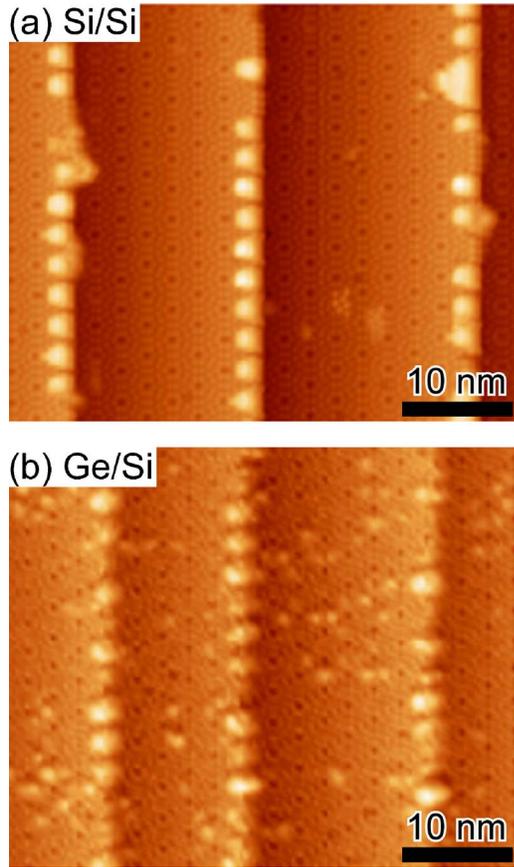
(a) Si/Si

10 nm

(b) Ge/Si

10 nm

FIG. 3. (Color online) STM images of the straight-step substrate partically covered with the Si and Ge nanoclusters. The growth conditions are (a) T_s =300 °C and w_{Si}=7b(Θ_{Si}=0.097 BL, θ=0.75°), (b) T_s=250 °C and w_{Ge} =7b(Θ_{Si}=0.13 BL, θ=1.0°). The nanocluster ordering at the upper step edges are better for the Si growth than for the Ge growth and the clusters on the terraces are only seen on the Ge-covered surface.
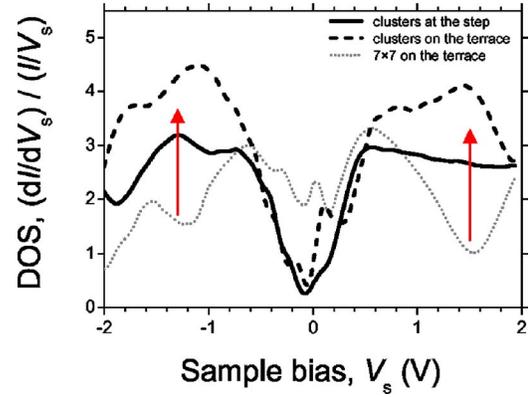

FIG. 4. (Color online) Room temperature STS spectra of the Ge nanocluster at the upper step edge (solid line), the Ge nanocluster on the terrace (dashed line), and the intact 7×7 structure on the same terrace (dotted line). The growth condition is as follows: T_s=250 °C, w_{Ge}=7b(Θ_{Ge}=0.13 BL, R =0.05 BL/min). The arrows at V_s≈−1.3 V and V_s≈+1.5 V indicate the localized electronic states of the Ge clusters.

unfaulted halves at the upper step edge, forms a defective 7×7 structure, on which the nucleation of Si and Ge is easier.

In the case of room temperature deposition of Si and Ge (T_s≈20 °C and w=7b), we observed only atomic protrusions or clusters on the terraces. Therefore, the room temperature is too low for Si and Ge atoms deposited on the terraces to reach the steps even with the small step-step distance (24 nm on average for θ=0.75°).

The growth behavior of Si and Ge is essentially the same at temperatures above 300 °C. However, we find notable differences at T_s≤300 °C. Figure 3 shows STM images with (a) deposited Si, w_{Si}=7b and T_s=300 °C and (b) deposited Ge, w_{Ge}=7b and T_s=250 °C. The 1D arrays of the nanoclusters along the step edges are seen in both images, as shown in Fig. 2(e). However, the Ge nanoclusters at the step edges are fewer and less ordered than those of Si. Moreover, only for the Ge growth smaller clusters are formed on the terraces. Increasing the nominal step coverage of Ge to 14b enhances the Ge nanocluster ordering but also leads to increasing number of the protrusions on the terraces. These differences cannot be attributed to the different diffusion lengths of Si and Ge atoms on the 7×7 surface, because the diffusion length of Ge is longer compared to Si.[32] We propose that the observed differences are due to the intermixing

of deposited Ge atoms and substrate Si atoms.[24] In the case of such an elevated temperature (T_s≥250 °C) and a small step-step distance (around 24 nm for θ=0.75°), most of Ge atoms adsorbed on the substrate will migrate on the 7×7 terraces and can reach the step edges. However, according to Wang *et al.*,[31] part of adsorbed Ge atoms can substitute Si adatoms in the 7×7 structure and are trapped in the adatom sites S_4. Then, the substituted Si atoms could migrate on the terrace and reach the step edges and, as well as the Ge atoms without substitution, incorporate into the nanoclusters at the step edges. In this way, the smallest protrusions on the terraces in the STM image should be the residual Ge adatoms, which may serve as nucleation centers for the cluster growth, and the nanoclusters at step edges might be a mixture of Ge and Si atoms.

We investigated the electronic structure of the Ge nanoclusters by STS.[24] Figure 4 shows STS spectra of the Ge nanoclusters at the step edge (solid line) and on the terrace (dashed) along with that of the intact 7×7 structure on the same terrace (dotted). The clean terrace spectrum exhibits the well-known features characteristic to the STS spectrum of the 7×7 surface at room temperature:[33] a significant density of states (DOS) at the sample Fermi level (sample bias voltage V_s≈0 V) and two broad maxima at V_s≈−0.6 V and ≈+0.5 V. The two spectra of the Ge nanoclusters are very similar to each other but distinctly different from the clean 7×7 spectrum. The DOS of the Ge nanoclusters is significantly decreased between V_s≈−0.3 V and ≈+0.2 V and increased at V_s≈−1.3 V and ≈+1.5 V. The decrease around the Fermi level can be attributed to the saturation of the adatom dangling bond states of the 7×7 surface by the Ge atoms in the nanoclusters, because these states dominate the 7×7 DOS around the Fermi level.[33] Similarly, we attribute the increase of the DOS at V_s≈−1.3 V and V_s≈+1.5 V to the modified surface DOS in the presence of the Ge atoms. From the size and shape of the Ge nanoclusters, we can conclude that they contain less than ten atoms.[34] Thus, we cannot ascribe the localized states of the Ge nanoclusters to the quantum confinement of free charge carriers inside the nanoclusters.[35]

IV. CONCLUSION

We have presented the unified description of the Si and Ge growth on the Si(111) surface with atomically straight step edges and the optimized method to prepare such highly ordered surface. We demonstrate that the optimum time of the kink-up dc annealing at 830 °C to extend the straight steps is about 10 h for the miscut of $\theta \approx 1°$ and $\phi \approx 3°$. Si and Ge exhibit the similar growth behavior: At the very beginning of the growth at the substrate temperature between 250 and 400 °C, the single-adatom-row nanowire structure (0.67 nm in width) is formed in a self-limited way due to the well-defined step-edge structure $U(2, 0)$; In subsequent growth of Si and Ge below 300 °C, the nanoclusters (narrower than 2.0 nm) are self-assembled in a 1D array (with 2.67 nm periodicity) along the upper step edge, because the pregrown atomic wire initiates their nucleation and promotes their growth. However, there are notable differences in the nanocluster growth below 300 °C: For the Ge growth, the nanoclusters at the steps are less ordered, and, additionally, the nanoclusters form also on the terraces. These differences can be explained by substitution of the substrate Si adatoms with deposited Ge. STS study reveals localized electronic states on the Ge nanoclusters.

ACKNOWLEDGMENTS

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