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Fabrication of Ge MOS with low interface trap density by ALD of Al_2O_3 on epitaxially grown Ge

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Abstract

Effects of initial surface conditions on interface characteristics of Al_2O_3/GeOx/Ge gate stacks are studied. As a clean surface condition prior to atomic layer deposition (ALD), a non-terminated Ge surface is realized by the insertion of an epitaxial Ge layer are grown on a Ge substrates in a MBE chamber which is directly connected to an ALD chamber. For these structures, the fixed charge density (Q_f) and interface trap density (D_{it}) are evaluated from the *C-V* characteristics and conductance method. Q_f reduction of about 17% and 90% are achieved by insertion of the epi-Ge layer and additional GeOx formation using plasma post-oxidation, respectively. A 90% reduction of D_{it} is also confirmed. These results indicate the importance of the initial Ge surface conditions before ALD and the Al_2O_3/GeOx/Ge gate stacks are very promising for high mobility Ge based CMOS applications.

Keywords: Ge, Al_2O_3, epitaxy, interface, trap, CV

(Some figures may appear in colour only in the online journal)

1. Introduction

To realize further improvements in CMOS performance, different channel materials with higher carrier mobility are required. Germanium is expected to be such a channel material because of its high mobility of both electrons (3900 $cm^2 V^{-1}s^{-1}$) and holes (1900 $cm^2 V^{-1}s^{-1}$) which are two and four times higher than those in Si [1]. For high performance Ge MOS devices, a high quality MOS interface is indispensable to realize high inversion carrier mobilities [2].

As one of the most conventional materials for Ge gate stacks, GeO_2 has been intensively studied in terms of interfacial properties and oxidization phenomena [3, 4]. Thermally grown GeO_2 gate stacks can sufficiently passivate the Ge MOS interface and reduce the interface trap density (D_{it}) $\sim 2 \times 10^{11}$ $eV^{-1}cm^{-2}$ (at E_i -0.2 eV, measured at 200 K) [5]. However, the Ge/GeO_2 interface is generally considered to be more defective than the Si/SiO_2 interface [6]. It was reported that the mobility of Ge MOSFETs with GeO_2 gate stacks followed the $\mu \propto 1/D_{it}$ relation [7], which indicated that the dominant mobility suppression mechanism is interface trap induced scattering. In addition, a GeO_2 film is not suitable for conventional CMOS technologies because of its unstable properties in atmosphere and its solubility to water.

From the viewpoint of the scaling limitations of CMOS technology, high-k gate insulators are required to achieve both lower equivalent oxide thickness (EOT) and suppression of tunnel gate leakage. Among various high-k gate insulators, Al_2O_3 insulators deposited by the atomic layer deposition (ALD) method are widely used to form high-quality gate stacks. However, defects are easily generated between the Al_2O_3/Ge interface [2] contrary to the Al_2O_3/Si high quality

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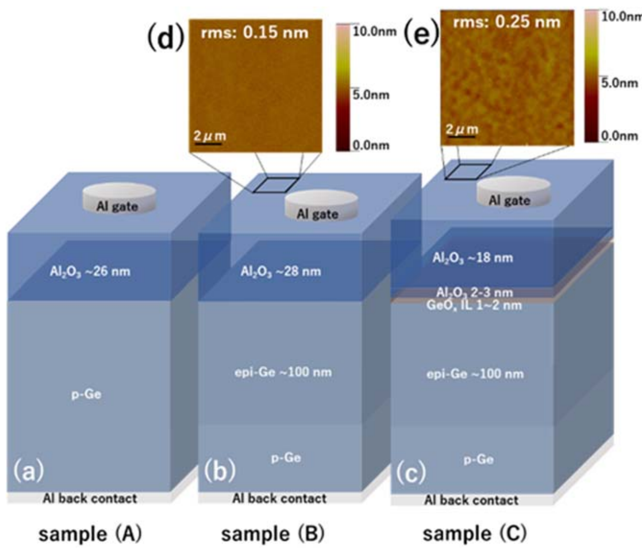

Figure 1. Schematic drawings of the MOS structures of the samples (a) (A), (b) (B) and (c) (C). Surface AFM images for the samples (d) (B) and (e) (C).

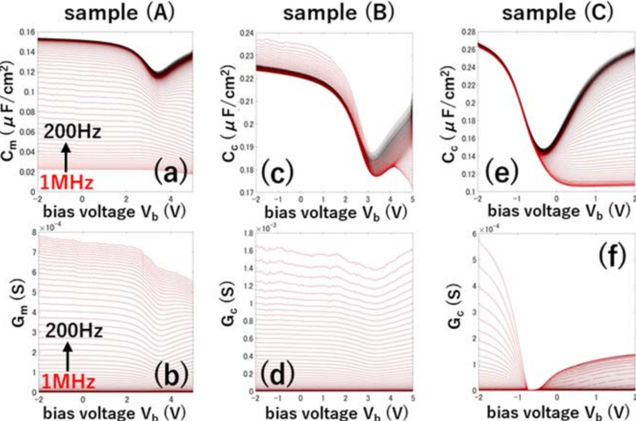

Figure 2. *C-V* and *G-V* plots of measured capacitance and conductance with frequencies from 200 Hz to 1 MHz corresponding to black to red curves, for the samples (A–C).

interface ($D_{it} \sim 10^{11}\ eV^{-1}cm^{-2}$, measured at room temperature [8]).

It is known that Al_2O_3 layers can be deposited by ALD only on OH-terminated surfaces [9]. Therefore, H-terminated and impurity contaminated Ge surface conditions inevitably cause growth defects.

To reduce these ALD defects, several approaches to control interface properties have been reported. One of the most promising methods is the plasma post-oxidization (PPO) method. A thin (0.5 ∼ 1 nm) GeOx interfacial layer (IL) is generated at the interface between Ge and Al_2O_3 by oxygen plasma irradiation after the deposition of a thin Al_2O_3 layer [10].

In this study, the effects of initial surface conditions on interface characteristics are investigated by evaluating fixed charge density (Q_f) and interface trap density (D_{it}) by means of *C-V* characteristics and conductance method.

2. Experimental methods

In this study, three types of Ge MOS capacitors were fabricated and named as samples (A), (B) and (C), as shown in figure 1. Firstly, p-Ge substrates (1–10 Ωcm) were chemically cleaned by NH_4OH solution followed by a de-ionized water rinse and 10% HF dip. After the chemical cleaning, sample (A) was loaded into the ALD chamber and a 26 nm thick Al_2O_3 film was deposited by 300 cycles of ALD at 300 °C substrate temperature with precursors of H_2O and $Al(CH_3)_3$. For samples (B) and (C), the cleaned Ge substrates were loaded into the MBE chamber followed by 800 °C pre-deposition baking for 20 min to remove surface H atoms. Then, 100 nm thick Ge buffer layers were epitaxially grown at 350 °C substrate temperature and non-terminated Ge surfaces were formed. Subsequently, the as-grown substrates were directly transferred to the vacuum-connected ALD chamber without atmospheric exposure. For sample (B), 28 nm Al_2O_3 was deposited on the epi-Ge surface with the same ALD deposition conditions as sample (A). For sample (C), only 2–3 nm (10 cycles of ALD) Al_2O_3 was deposited on the epi-Ge surface for the next plasma irradiation process to form a plasma-induced GeOx interfacial layer (IL). Then, sample (C) was transferred to the PECVD chamber to perform PPO. By the irradiation of oxygen plasma for 15 s, 1 ∼ 2 nm of GeOx IL was generated between the epi-Ge layer and Al_2O_3 at substrate temperature of 300 °C. After the PPO, a further 200 cycles of ALD was performed to form an 18 nm Al_2O_3 film to avoid leakage during CV measurements. Then, post-deposition annealing (PDA) was performed at 450 °C in N_2 ambient for 30 min for all the samples. Finally, Al gate electrodes ($\sim 3 \times 10^{-3}\ cm^2$) and back contacts were deposited by thermal evaporation.

The *C-V* and *G-V* measurements were performed at room temperature by using an Agilent E4980A LCR meter. The fixed charge density (Q_f) was evaluated from *C-V* characteristics and interface trap density (D_{it}) was evaluated by using the conductance method in the range from flat band to weak inversion states. The series resistance and capacitance correction (SRCC) method [11, 12] was applied to the conductance method to handle the hetero impedance of the epitaxially grown intrinsic Ge layer.

3. Results and discussions

3.1. Sample surface condition

The sample surface conditions were observed by AFM as shown in figures 1(d) and (e). The surface root mean square roughness is ∼0.15 nm for the sample (B) and 0.25 nm for the sample (C), which indicates that high quality Ge epitaxial grown layers were obtained with sufficiently flat surfaces for accurate *C-V* measurements.

3.2. C-V, G-V measurements

Measured *C-V* and *G-V* characteristics of the samples (A-C) are shown in figure 2. In figures 2(a), (b), the measured capacitance (C_m) and measured conductance (G_m) from

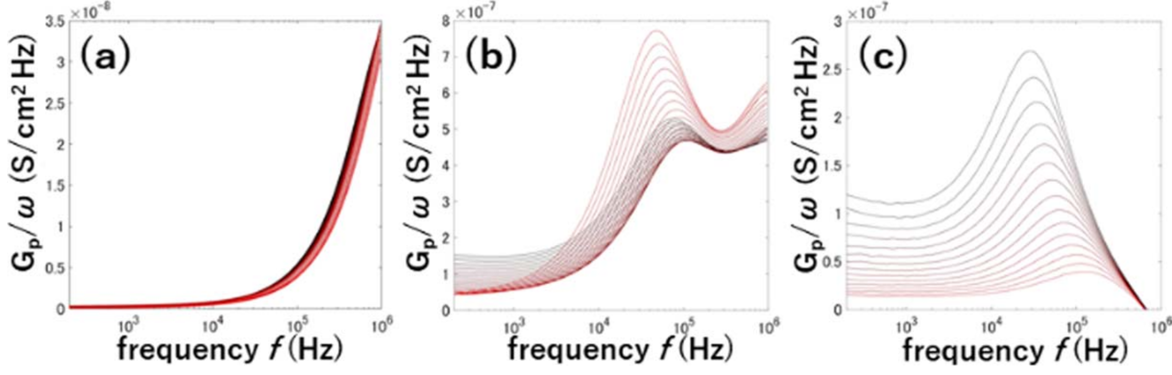

Figure 3. G_p/ω-f plots at specific bias voltages V_b from flat band state to weak inversion state of samples (A–C).

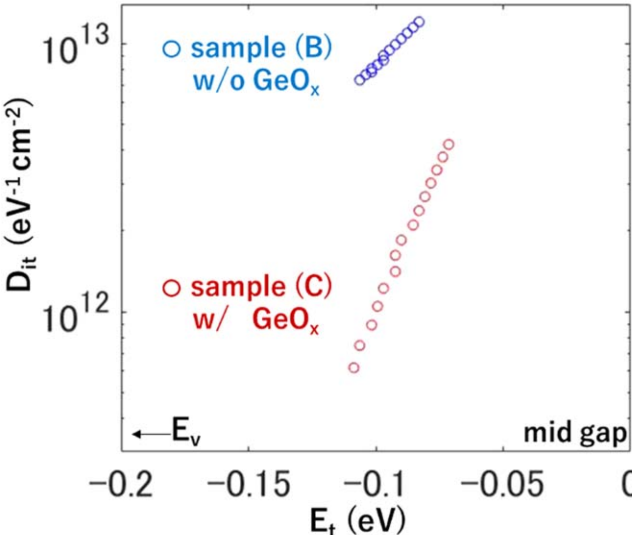

Figure 4. Energy distributions of D_{it}. Two kinds of D_{it} distributions are plotted from samples (B) and (C). The blue plots show D_{it} of sample (B), red plots show D_{it} of sample (C).

sample (A) are shown. For the samples with epi-Ge layers (samples (B) and (C)), SRCC were applied by using equation (1) [12] to handle the hetero impedance of the intrinsic Ge layer.

$$C_c = \frac{C_m(\omega^2 C_h^2 + G_h^2) - C_h(\omega^2 C_m^2 + G_m^2)}{(G_h - G_m)^2 + \omega^2 (C_h - C_m)^2} \quad (1)$$

As a result, the corrected capacitance (C_c) was obtained as shown in figures 2(c), (e). Similarly, the corrected conductance (G_c) was obtained by using the SRCC model (equation (2) [12]).

$$G_c = \frac{G_m(\omega^2 C_h^2 + G_h^2) - G_h(\omega^2 C_m^2 + G_m^2)}{(G_h - G_m)^2 + \omega^2 (C_h - C_m)^2} \quad (2)$$

In the *C-V* and *G-V* measurements, frequency (f) was swept form 200 Hz to 1 MHz at the specific 100 points of bias voltages (V_b) corresponding to strong accumulation and strong inversion states. Typical *C-V* behaviors for a p-type MOS capacitor are observed, although an intrinsic Ge layer is epitaxially grown on the surface (figures 2(b), (c)). Concerning the capacitance of sample (A) shown in figure 2(a), large frequency dispersion of the capacitance is observed due to the defect induced series admittance. It is also observed that the conductance remarkably drops in the range from depletion to weak inversion for sample (C) (figure 2(f)), indicating the suppression of interface defects in this structure.

For further accurate analysis of these defects, Q_f and D_{it} are investigated.

Table 1. Fixed charge density Q_f of each sample calculated by using C_{ox} and V_{FB}. Al_2O_3 thickness d_{Al2O3} is measured by ellipsometry to determine C_{ox}.

Sample	d_{Al2O3} (nm)	$\phi - V_{FB}$ (V)	Q_f (cm^{-2})
Sample (A)	26	–4.1	–7.3 × 10^{12}
Sample (B)	28	–3.6	–6.1 × 10^{12}
Sample (C)	21	–0.3	–6.7 × 10^{11}

3.3. Fixed charge density Q_f

Q_f is expressed by equation (3) [13], where ϕ and V_{FB} are the work function difference and flat band voltage, respectively.

$$Q_f = (\phi - V_{FB}) C_{ox} \quad (3)$$

From the measured *C-V* curves (figure 2), C_{ox} can be determined experimentally from the measured thickness and V_{FB} can be also obtained from the flat band voltage shift in the high frequency C-V characteristics.

The obtained Q_f is $Q_f = -7.3 \times 10^{12}\,\mathrm{cm}^{-2}$ for sample (A), $Q_f = -6.1 \times 10^{12}\,\mathrm{cm}^{-2}$ for sample (B) and $Q_f = -6.7 \times 10^{11}\,\mathrm{cm}^{-2}$ for sample (C) as shown in table 1.

From this result, it is shown that Q_f is decreased almost 17% by the insertion of the impurity-free and non-terminated epitaxial Ge prior to Al_2O_3 deposition. Additionally, Q_f can be decreased over 90% by the insertion of GeOx IL by PPO due to the surface passivation effect of GeOx [5]. The absolute value of Q_f for sample (C) is almost the same level as the previously reported one from GeO_2 gate stacks (~6 × 10^{11} cm^{-2} [14]). Therefore, it can be said that improvements of interface characteristics and sufficiently impurity-free gate stacks can be realized by the Al_2O_3/GeOx/epi-Ge gate stack.

Table 2. The minimum D_{it} and D_{it} at a specific energy level (E_i −0.1 eV) of samples (A-C). There is no D_{it} value in sample (A) because no G_p/ω peak was observed, as shown in figure 3(a).

Sample	epi-Ge	GeO_x	min D_{it} ($eV^{-1}cm^{-2}$)	D_{it} at E_i–0.1 eV ($eV^{-1}cm^{-2}$)
Sample-A	×	×	—	—
Sample-B	○	×	7.3×10^{12}	8.0×10^{12}
Sample-C	○	○	6.2×10^{11}	8.9×10^{11}

3.4. Interface trap density Dit

For the further accurate evaluation of interfacial properties, the interface trap density D_{it} is investigated by using the conductance method [15]. D_{it} is deduced from simplified conductance (G_p) which is derived from equivalent circuits [15]. From the *C-f* and *G-f* measurements and SRCC correction as shown in figure 2, G_p/ω characteristics are obtained by using equation (4)

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{4}$$

where C_{ox}, C_m (=C_c) and G_m (=G_c) are oxide capacitance, measured capacitance and measured conductance, respectively, and $\omega = 2\pi f$.

Figure 3 shows G_p/ω-*f* plots at each bias voltage V_b corresponding to the range from flat band state to weak inversion state. For sample (A), there is no G_p/ω peak as shown in figure 3(a), making it impossible to obtain D_{it}. By comparing figures 3(b) and (c), the decrease in the peak intensity in figure 3(c) is observed in the similar peak frequency ranges. This characteristic suggests the reduction of D_{it} and improvements of the interface quality because the peak intensity is directly related to the D_{it} as predicted by equation (5).

$$D_{it} = \frac{2.5}{Aq^2} \frac{G_p}{\omega} \bigg|_{peak} \tag{5}$$

The D_{it} can be obtained by substituting the peak value of G_p/ω in figure 3 to equation (5). Finally, energy distributions of D_{it} were obtained as shown in figure 4.

For sample (A), it is impossible to evaluate D_{it} by the conductance method because of the low interface quality. On the other hand, for sample (B), D_{it} comparable with reported values in Ge/GeO_2 gate stacks ($\sim 3 \times 10^{12}\,eV^{-1}cm^{-2}$ at E_i −0.1 eV [3]) can be realized by the insertion of the epi-Ge layer. Benefits of the Al_2O_3/epi-Ge gate stacks are not only the reduction of surface impurities but also the improvement of ALD initial growth because the OH-terminated surface is easily formed in the first cycle of ALD on the dangling bonds covered surface.

The improvement in interface quality by insertion of the GeOx IL by PPO on the epi-Ge layer was also confirmed from the D_{it} distributions of samples (B) and (C) in figure 4. The minimum D_{it} and D_{it} at a specific energy level (E_i −0.1 eV) are obtained as shown in table 2. About one order of magnitude reduction of both minimum D_{it} (∼92% of reduction) and D_{it} at the specific energy level (∼89% of reduction) can be achieved. The surface passivation effect by the insertion of the GeOx IL by PPO have already been reported in the previous research which reported the 94% decrease of D_{it} (from $D_{it} = 1.9 \times 10^{12}\,eV^{-1}cm^{-2}$ to $D_{it} = 1.2 \times 10^{11}\,eV^{-1}cm^{-2}$ at E_i −0.2 eV) by performing PPO [16]. The obtained D_{it} value (at E_i −0.1 eV) for sample (C) is significantly lower than the reported D_{it} value at the same energy level and measurement temperature for GeO_2 gate stacks ($D_{it} \sim 3 \times 10^{12}\,eV^{-1}cm^{-2}$ at E_i −0.1 eV [3]).

4. Conclusion

MOS capacitors of Al_2O_3/GeOx/epi-Ge/Ge structure have been fabricated. We showed the improvements of interface characteristics by preparing a clean initial Ge surface prior to ALD and inserting GeOx IL by plasma post-oxidization (PPO).

As quality indicators of the interface, Q_f and D_{it} have been investigated from *C-V* characteristics.

By insertion of the epi-Ge layer prior to ALD, we achieved a 17% of Q_f reduction and D_{it} comparable to previously reported D_{it} in GeO_2/Ge gate stacks [3]. These improvements originate from impurity free surface conditions and dangling bond terminated surface conditions which are suitable to form OH-termination as an initial condition prior to ALD.

Similarly, by insertion of GeOx IL by PPO on the clean surface realized by insertion of the epi-Ge layer, 90% reduction of both Q_f and D_{it} was achieved because of the benefits of clean surface preparation and GeOx passivation effect. This obtained D_{it} value is significantly lower than D_{it} values reported in GeO_2 measured at the same temperature [3].

These results indicate the importance of initial Ge surface conditions prior to ALD in the Al_2O_3/GeOx/Ge gate stack.

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